MOTOROLA

MC34119

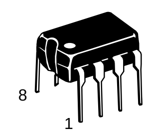
Low Power Audio Amplifier

The MC34119 is a low power audio amplifier intergrated circuit intended (primarily) for telephone applications, such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages (2.0 V minimum). Coupling capacitors to the speaker are not required. Open loop gain is 80 dB, and the closed loop gain is set with two external resistors. A Chip Disable pin permits powering down and/or muting the input signal. The MC34119 is available in standard 8–pin DIP, SOIC package, and TSSOP package.

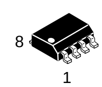
- Wide Operating Supply Voltage Range (2.0 V to 16 V), Allows Telephone Line Powered Applications
- Low Quiescent Supply Current (2.7 mA Typ) for Battery Powered Applications
- Chip Disable Input to Power Down the IC
- Low Power–Down Quiescent Current (65 µA Typ)
- Drives a Wide Range of Speaker Loads (8.0 Ω and Up)
- Output Power Exceeds 250 mW with 32 Ω Speaker
- Low Total Harmonic Distortion (0.5% Typ)
- Gain Adjustable from <0 dB to >46 dB for Voice Band
- Requires Few External Components

LOW POWER AUDIO AMPLIFIER

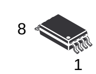
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



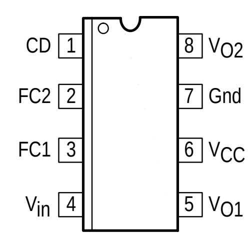
DTB SUFFIX
PLASTIC PACKAGE
CASE 948J
(TSSOP)

MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage	–1.0 to +18	Vdc
Maximum Output Current at V_{O1}, V_{O2}	±250	mA
Maximum Voltage @ V_{in}, FC1, FC2, CD Applied Output Voltage to V_{O1}, V_{O2} when disabled	–1.0, V_{CC} + 1.0 –1.0, V_{CC} + 1.0	Vdc
Junction Temperature	–55, +140	°C

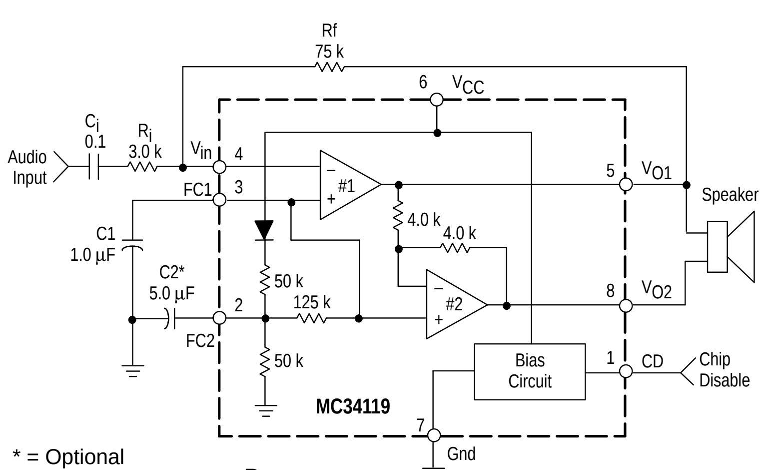
NOTE: ESD data available upon request.

PIN CONNECTIONS



(Top View)

Block Diagram and Simplified Application



* = Optional

Differential Gian = 2 x $\frac{R_f}{R_i}$

This device contains 45 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34119P	T_A = –20° to +70°C	Plastic DIP
MC34119D		SO–8
MC34119DTB		TSSOP

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Supply Voltage Voltage @ CD (Pin 1)	V_{CC} V_{CD}	+2.0 0	+16 V_{CC}	Vdc Vdc
Load Impedance	R_L	8.0	–	Ω
Peak Load Current	I_L	–	±200	mA
Differential Gain (5.0 kHz Bandwidth)	AVD	0	46	dB
Ambient Temperature	T_A	–20	+70	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
AMPLIFIERS (AC CHARACTERISTICS)					
AC Input Resistance (@ V_{In})	r_i	–	>30	–	MΩ
Open Loop Gain (Amplifier #1, f < 100 Hz)	A_{VOL1}	80	–	–	dB
Closed Loop Gain (Amplifier #2, V_{CC} = 6.0 V, f = 1.0 kHz, R_L = 32 Ω)	A_{V2}	–0.35	0	+0.35	dB
Gain Bandwidth Product	GBW	–	1.5	–	MHz
Output Power; V_{CC} = 3.0 V, R_L = 16 Ω, THD ≤ 10% V_{CC} = 6.0 V, R_L = 32 Ω, THD ≤ 10% V_{CC} = 12 V, R_L = 100 Ω, THD ≤ 10%	 P_{Out3} P_{Out6} P_{Out12}	 55 250 400	 – – –	 – – –	mW
Total Harmonic Distortion (f = 1.0 kHz) (V_{CC} = 6.0 V, R_L = 32 Ω, P_{out} = 125 mW) (V_{CC} ≥ 3.0 V, R_L = 8.0 Ω, P_{out} = 20 mW) (V_{CC} ≥ 12 V, R_L = 32 Ω, P_{out} = 200 mW)	THD	 – – –	 0.5 0.5 0.6	 1.0 – –	%
Power Supply Rejection (V_{CC} = 6.0 V, ΔV_{CC} = 3.0 V) (C1 = ∞, C2 = 0.01 µF) (C1 = 0.1 µF, C2 = 0, f = 1.0 kHz) (C1 = 1.0 µF, C2 = 5.0 µF, f = 1.0 kHz)	PSRR	 50 – –	 – 12 52	 – – –	dB
Differential Muting (V_{CC} = 6.0 V, 1.0 kHz ≤ f ≤ 20 kHz, CD = 2.0 V)	GMT	–	>70	–	dB
AMPLIFIERS (DC CHARACTERISTICS)					
Output DC Level @ V_{O1}, V_{O2}, V_{CC} = 3.0 V, R_L = 16 (R_f = 75 k) V_{CC} = 6.0 V V_{CC} = 12 V	$V_{O(3)}$ $V_{O(6)}$ $V_{O(12)}$	1.0 – –	1.15 2.65 5.65	1.25 – –	Vdc
Output Level High (I_{out} = –75 mA, 2.0 V ≤ V_{CC} ≤ 16 V) Low (I_{out} = 75 mA, 2.0 V ≤ V_{CC} ≤ 16 V)	 V_{OH} V_{OL}	 – –	 V_{CC} – 1.0 0.16	 – –	Vdc
Output DC Offset Voltage (V_{O1}–V_{O2}) (V_{CC} = 6.0 V, R_f = 75 kΩ, R_L = 32 Ω)	ΔV_O	 –30	 0	 +30	mV
Input Bias Current @ V_{in} (V_{CC} = 6.0 V)	I_{IB}	–	–100	–200	nA
Equivalent Resistance @ FC1 (V_{CC} = 6.0 V) @ FC2 (V_{CC} = 6.0 V)	 R_{FC1} R_{FC2}	 100 18	 150 25	 220 40	kΩ
CHIP DISABLE (Pin 1)					
Input Voltage Low High	 V_{IL} V_{IH}	 – 2.0	 – –	 0.8 –	Vdc
Input Resistance (V_{CC} = V_{CD} = 16 V)	R_{CD}	50	90	175	kΩ
POWER SUPPLY					
Power Supply Current (V_{CC} = 3.0 V, R_L = ∞, CD = 0.8 V) (V_{CC}= 16 V, R_L = ∞, CD = 0.8 V) (V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)	 I_{CC3} I_{CC16} I_{CCD}	 – – –	 2.7 3.3 65	 4.0 5.0 100	 mA mA µA

NOTE: Currents into a pin are positive, currents out of a pin are negative.

PIN FUNCTION DESCRIPTION

Symbol	Pin	Description
CD	1	Chip Disable – Digital input. A Logic “0” (<0.8 V) sets normal operation. A logic “1” (≥2.0 V) sets the power down mode. Input impedance is nominally 90 kΩ .
FC2	2	A capacitor at this pin increases power supply rejection, and affects turn–on time. This pin can be left open if the capacitor at FC1 is sufficient.
FC1	3	Analog ground for the amplifiers. A 1.0 µF capacitor at this pin (with a 5.0 µF capacitor at Pin 2) provides (typically) 52 dB of power supply rejection. Turn–on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input.
V_{in}	4	Amplifier input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and V_{O1}.
V_{O1}	5	Amplifier Output #1. The dc level is ≈ (V_{CC} – 0.7 V)/2.
V_{CC}	6	DC supply voltage (+2.0 V to +16 V) is applied to this pin.
GND	7	Ground pin for the entire circuit.
V_{O2}	8	Amplifier Output #2. This signal is equal in amplitude, but 180° out–of–phase with that at V_{O1}. The dc level is ≈ (V_{CC} – 0.7 V)/2.

TYPICAL TEMPERATURE PERFORMANCE (–20° C < T_A < +70°C)

Function	Typical Change	Units
Input Bias Current (@ V_{in})	±40	pA/°C
Total Harmonic Distortion (V_{CC} = 6.0 V, R_L = 32 Ω. P_{out} = 125 mW, f = 1.0 kHz)	+0.003	%/°C
Power Supply Current (V_{CC} = 3.0 V, R_L = ∞, CD = 0 V) (V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)	 –2.5 –0.03	µA/°C

DESIGN GUIDELINES

General

The MC34119 is a low power audio amplifier capable of low voltage operation (V_{CC} = 2.0 V minimum) such as that encountered in line–powered speakerphones. The circuit provides a differential output (V_{O1}–V_{O2}) to the speaker to maximize the available voltage swing at low voltages. The differential gain is set by two external resistors. Pins FC1 and FC2 allow controlling the amount of power supply and noise rejection, as well as providing alternate inputs to the amplifiers. The CD pin permits powering down the IC for muting purposes and to conserve power.

Amplifiers

Referring to the block diagram, the internal configuration consists of two identical operational amplifiers. Amplifier #1 has an open loop gain of ≥80 dB (at f ≤ 100 Hz), and the closed loop gain is set by external resistor R_f and R_i. The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5 MHz. In order to adequately cover the telephone voice band (300 Hz to 3400 Hz), a maximum closed loop gain of 46 is recommended. Amplifier #2 is internally set to a gain of – 1.0 (0 dB).

The outputs of both amplifiers are capable of sourcing and sinking a peak current of 200 mA. The outputs can typically swing to within ≈0.4 V above ground, and to within ≈1.3 V below V_{CC}, at the maximum current. See Figures 18 and 19 for V_{OH} and V_{OL} curves.

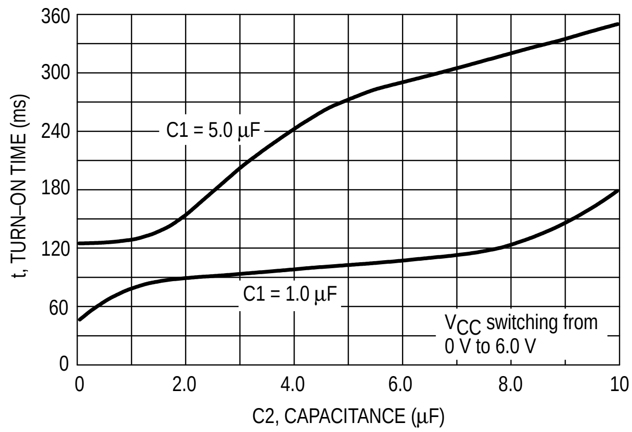
The output dc offset voltage (V_{O1}–V_{O2}) is primarily a function of the feedback resistor (R_f), and secondarily due to the amplifiers' input offset voltages. The input offset voltage of the two amplifiers will generally be similar for a particular IC, and therefore nearly cancel each other at the outputs. Amplifier #1's bias current, however, flows out of V_{in} (Pin 4) and through R_f, forcing V_{O1} to shift negative by an amount equal to [$R_f \times I_{IB}$]. V_{O2} is shifted positive an equal amount. The output offset voltage, specified in the Electrical Characteristics, is measured with the feedback resistor shown in the Typical Application Circuit, and therefore takes into account the bias current as well as internal offset voltages of the amplifiers. The bias current is constant with respect to V_{CC}.

FC1 and FC2

Power supply rejection is provided by the capacitors (C1 and C2 in the Typical Application Circuit) at FC1 and FC2. C2 is somewhat dominant at low frequencies, while C1 is dominant at high frequencies, as shown in the graphs of Figures 4 to 7. The required values of C1 and C2 depend on the conditions of each application. A line powered speakerphone, for example, will require more filtering than a circuit powered by a well regulated power supply. The amount of rejection is a function of the capacitors, and the equivalent impedance looking into FC1 and FC2 (listed in the Electrical Characteristics as R_{FC1} and R_{FC2}).

In addition to providing filtering, C1 and C2 also affect the turn–on time of the circuit at power–up, since the two capacitors must charge up through the internal 50 k and 125 kΩ resistors. The graph of Figure 1 indicates the turn–on time upon application of V_{CC} of +6.0 V. The turn–on time is ≈60% longer for V_{CC} = 3.0 V, and ≈20% less for V_{CC} = 9.0 V. Turn–off time is <10 µs upon removal of V_{CC}.

Figure 1. Turn–On Time versus C1, C2 at Power–On



Chip Disable

The Chip Disable (Pin 1) can be used to power down the IC to conserve power, or for muting, or both. When at a Logic "0" (0 V to 0.8 V), the MC34119 is enabled for normal operation. When Pin 1 is at a Logic "1" (2.0 V to V_{CC} V), the IC is disabled. If Pin 1 is open, that is equivalent to a Logic "0," although good design practice dictates that an input should never be left open. Input impedance at Pin 1 is a nominal 90 kΩ. The power supply current (when disabled) is shown in Figure 15.

Muting, defined as the change in differential gain from normal operation to muted operation, is in excess of 70 dB. The turn–off time of the audio output, from the application of the CD signal, is <2.0 µs, and turn on–time is 12 ms–15 ms. Both times are independent of C1, C2, and V_{CC}.

When the MC34119 is disabled, the voltages at FC1 and FC2 do not change as they are powered from V_{CC}. The outputs, V_{O1} and V_{O2}, change to a high impedance condition, removing the signal from the speaker. If signals from other sources are to be applied to the outputs (while disabled), they must be within the range of V_{CC} and Ground.

Power Dissipation

Figures 8 to 10 indicate the device dissipation (within the IC) for various combinations of V_{CC}, R_L, and load power. The maximum power which can safely be dissipated within the MC34119 is found from the following equation:

$$P_D = (140°C - T_A)/\theta_{JA}$$

where T_A is the ambient temperature; and θ_{JA} is the package thermal resistance (100°C/W for the standard DIP package, and 180°C/W for the surface mount package.)

The power dissipated within the MC34119, in a given application, is found from the following equation:

$$P_D = (V_{CC} \times I_{CC}) + (I_{RMS} \times V_{CC}) - (R_L \times I_{RMS}^2)$$

where I_{CC} is obtained from Figure 15; and I_{RMS} is the RMS current at the load; and R_L is the load resistance.

Figures 8 to 10, along with Figures 11 to 13 (distortion curves), and a peak working load current of ±200 mA, define the operating range for the MC34119. The operating range is further defined in terms of allowable load power in Figure 14 for loads of 8.0 Ω, 16 Ω and 32 Ω. The left (ascending) portion

of each of the three curves is defined by the power level at which 10% distortion occurs. The center flat portion of each curve is defined by the maximum output current capability of the MC34119. The right (descending) portion of each curve is defined by the maximum internal power dissipation of the IC at 25°C. At higher ambient temperatures, the maximum load power must be reduced according to the above equations. Operating the device beyond the current and junction temperature limits will degrade long term reliability.

Layout Considerations

Normally a snubber is not needed at the output of the MC34119, unlike many other audio amplifiers. However, the PC board layout, stray capacitances, and the manner in which the speaker wires are configured, may dictate otherwise. Generally, the speaker wires should be twisted tightly, and not more than a few inches in length.

Figure 2. Amplifier #1 Open Loop Gain and Phase

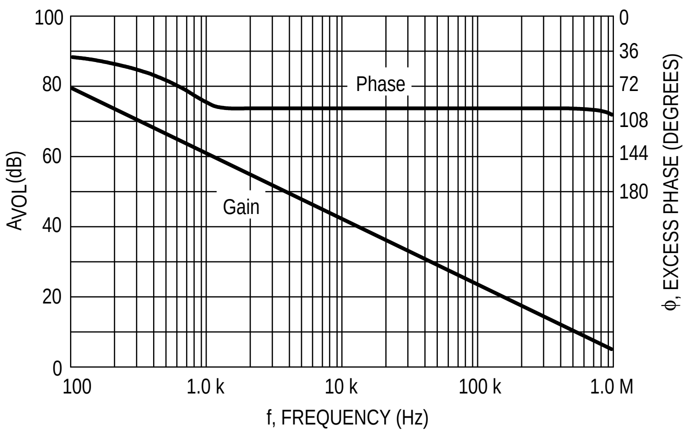


Figure 3. Differential Gain versus Frequency

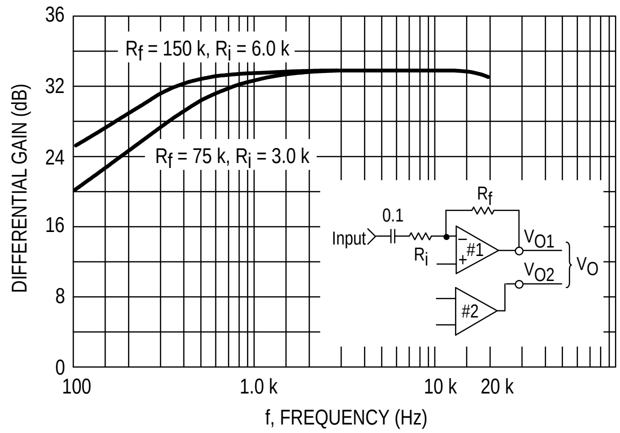


Figure 4. Power Supply Rejection versus Frequency (C2 = 10 µF)

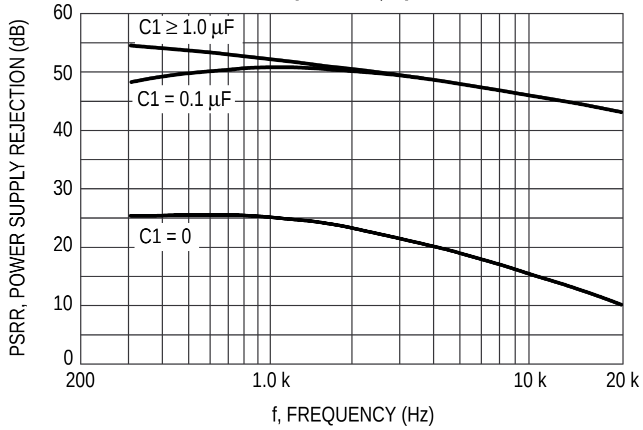


Figure 5. Power Supply Rejection versus Frequency (C2 = 5.0 µF)

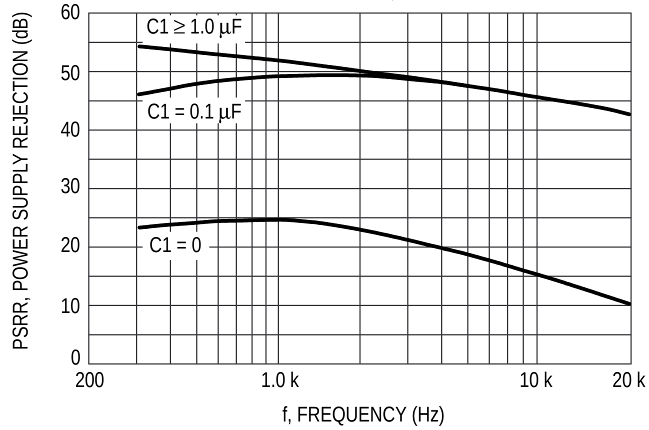


Figure 6. Power Supply Rejection versus Frequency (C2 = 1.0 µF)

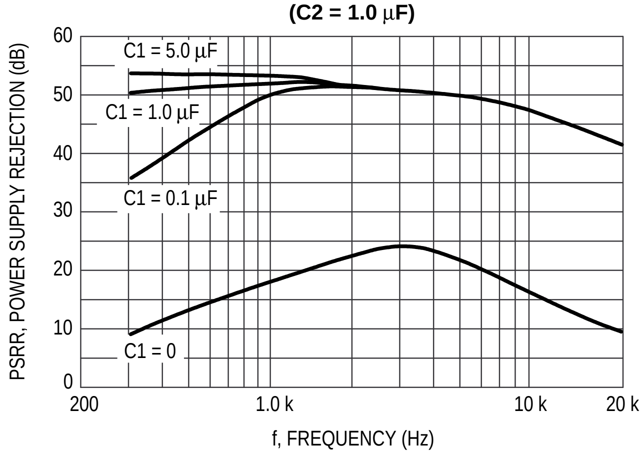


Figure 7. Power Supply Rejection versus Frequency (C2 = 0)

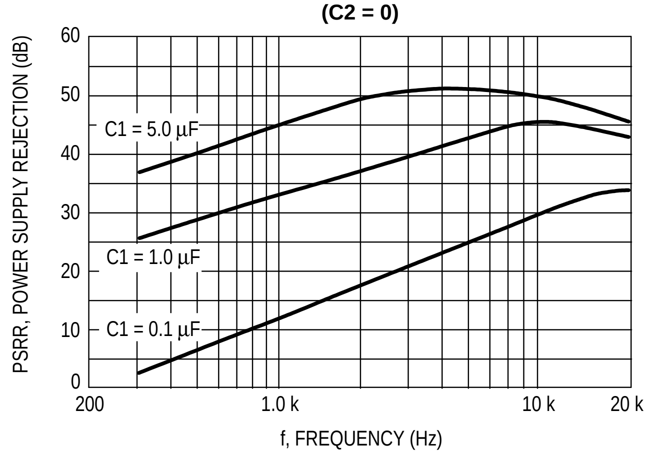


Figure 8. Device Dissipation, 8.0 Ω Load

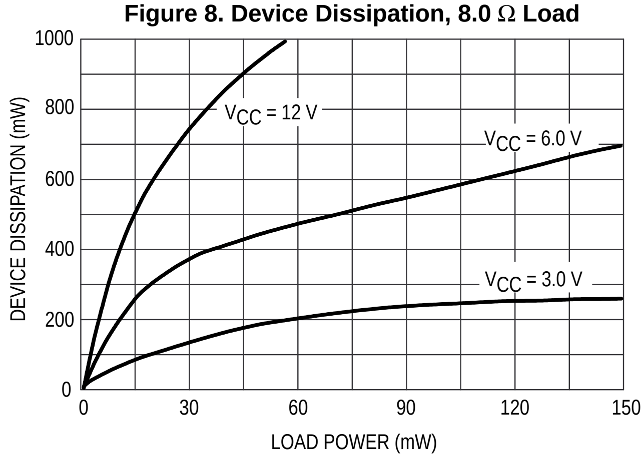


Figure 9. Device Dissipation, 16 Ω Load

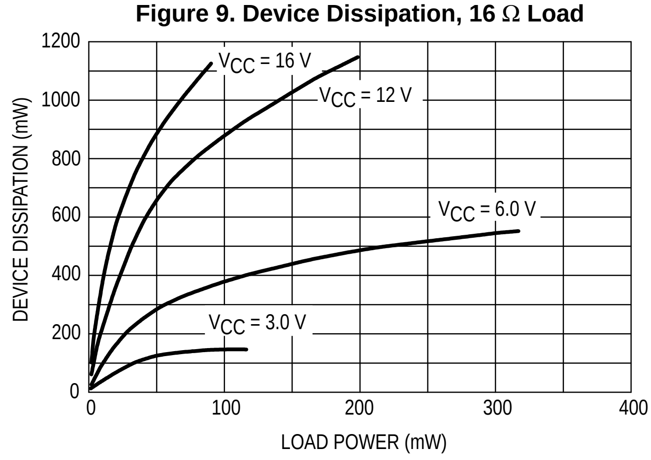


Figure 10. Device Dissipation, 32 Ω Load

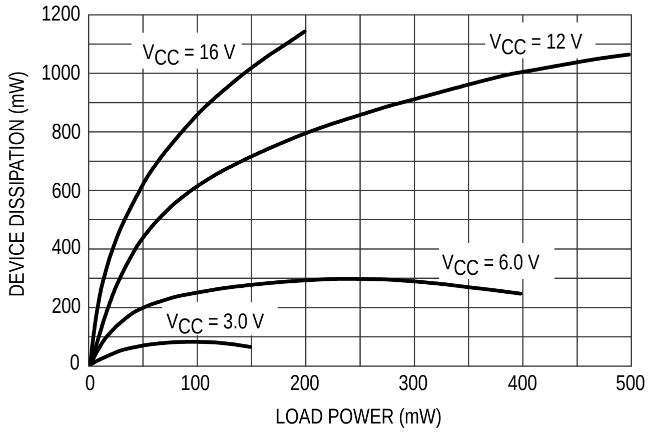


Figure 11. Distortion versus Power
(f = 1.0 kHz, AVD = 34 dB)

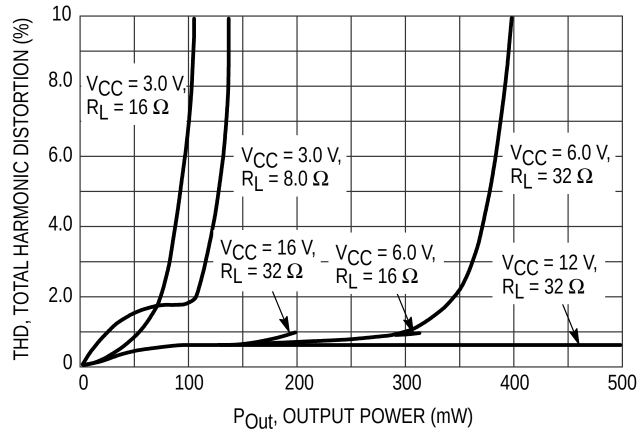


Figure 12. Distortion versus Power
(f = 3.0 kHz, AVD = 34 dB)

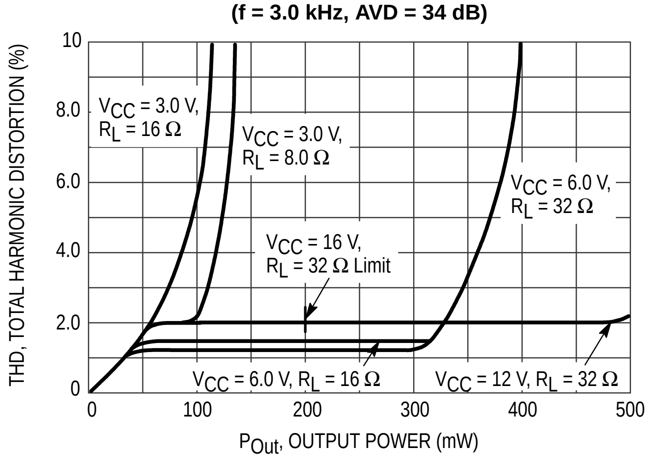


Figure 13. Distortion versus Power
(f = 1, 3.0 kHz, AVD = 12 dB)

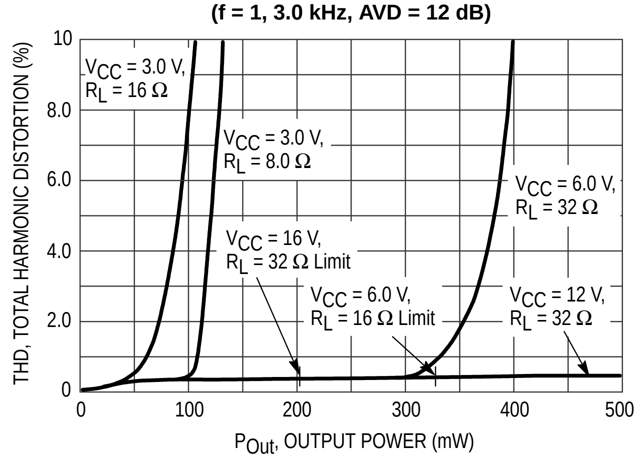


Figure 14. Maximum Allowable Load Power

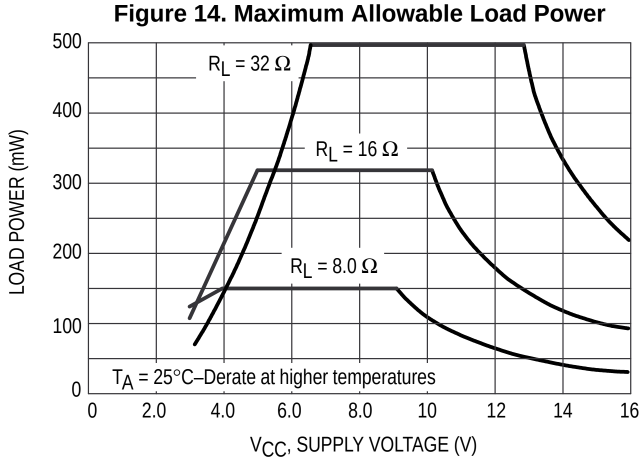
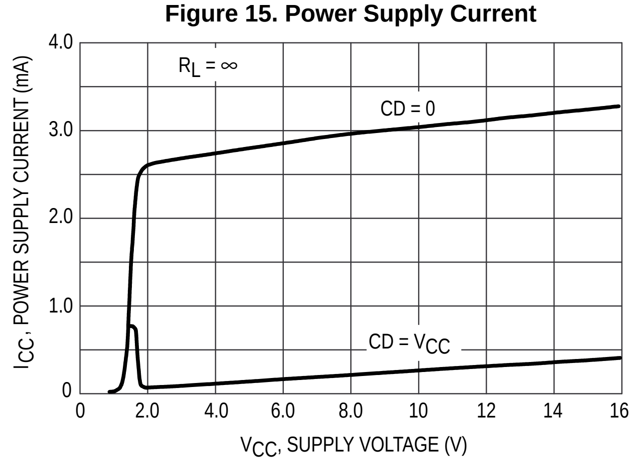


Figure 15. Power Supply Current



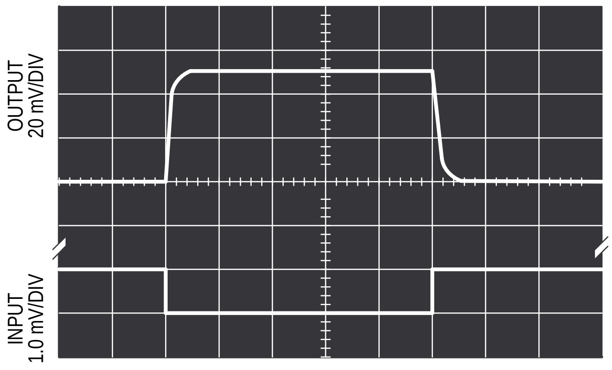


Figure 16. Small Signal Response

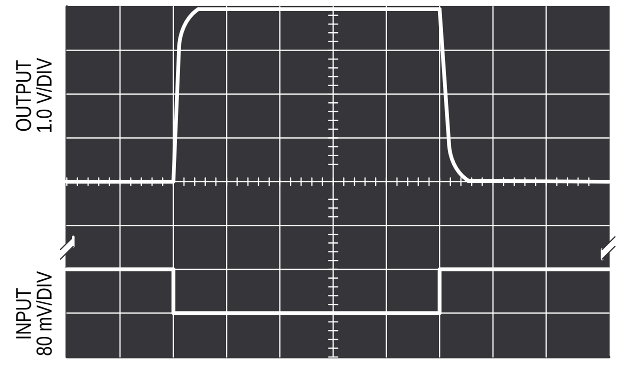


Figure 17. Large Signal Response

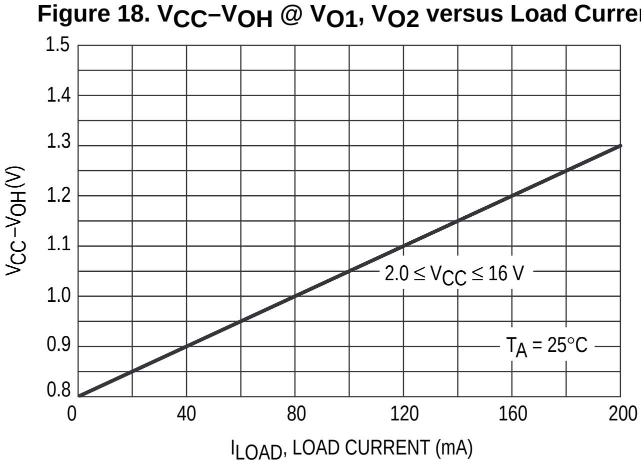


Figure 18. $V_{CC}-V_{OH}$ @ V_{O1}, V_{O2} versus Load Current

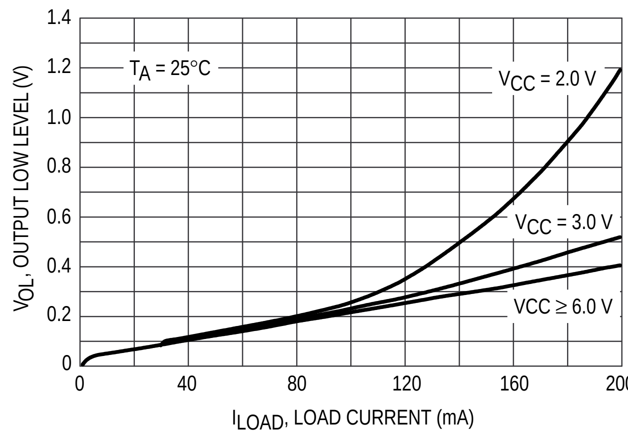


Figure 19. V_{OL} @ V_{O1}, V_{O2} versus Load Current

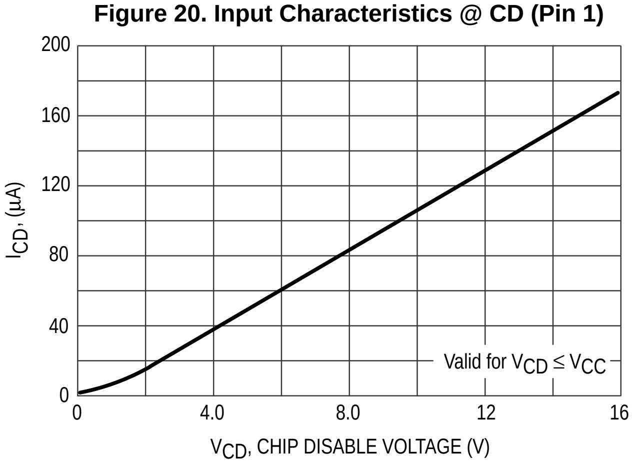


Figure 20. Input Characteristics @ CD (Pin 1)

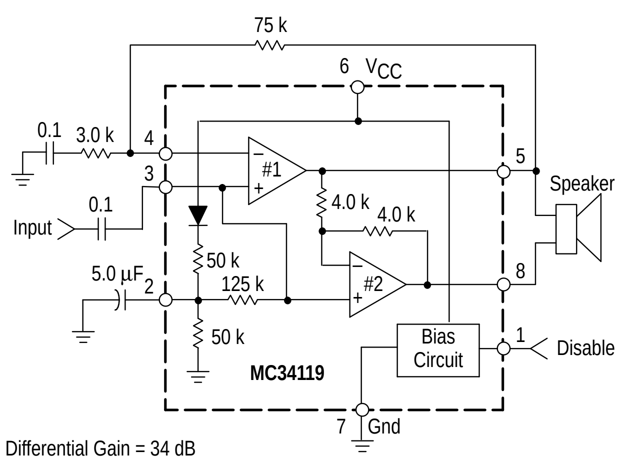


Figure 21. Audio Amplifier with High Input Impedance

Differential Gain = 34 dB
Frequency Response: See Figure 3
Input Impedance ≈ 125 kΩ
PSRR ≈ 50 dB

Figure 22. Audio Amplifier with Bass Suppression

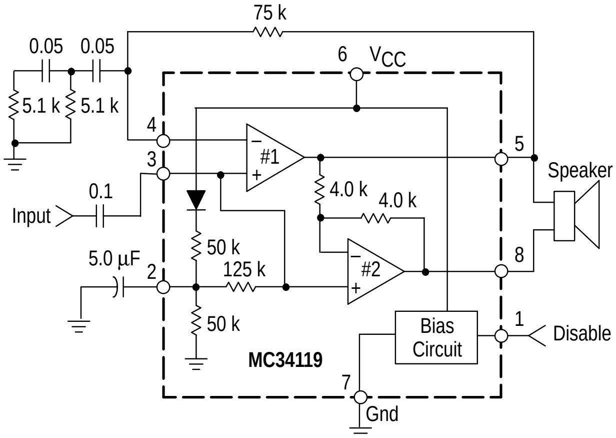


Figure 23. Frequency Response of Figure 22

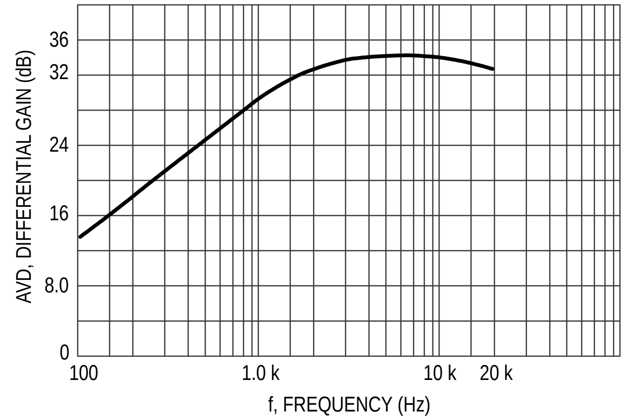


Figure 24. Audio Amplifier with Bandpass

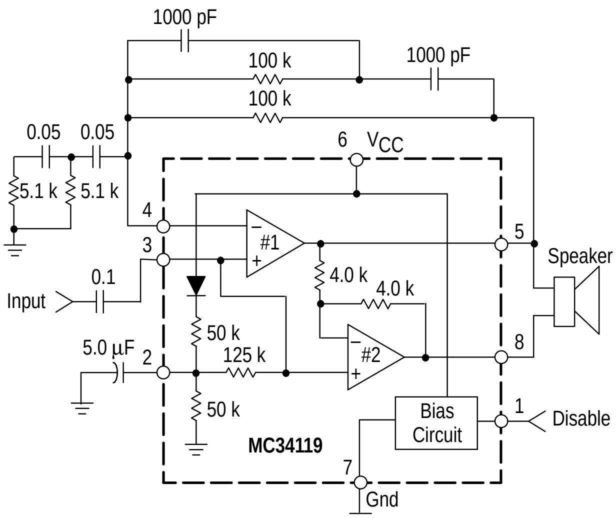


Figure 25. Frequency Response of Figure 24

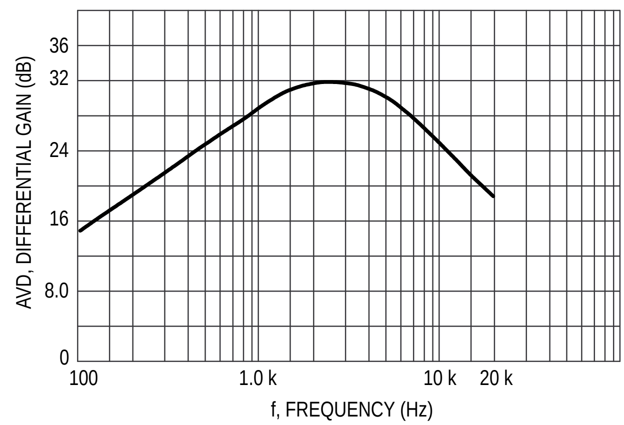
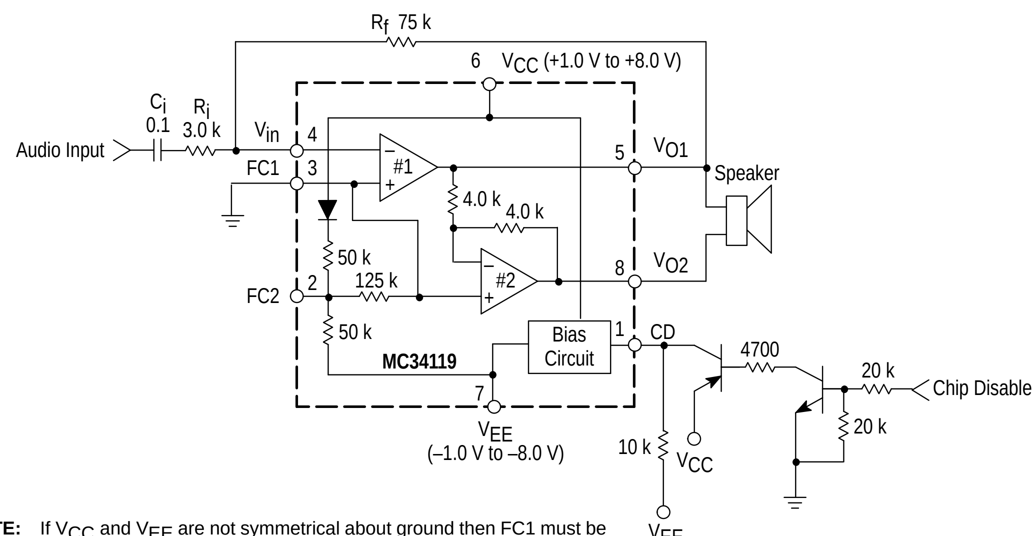


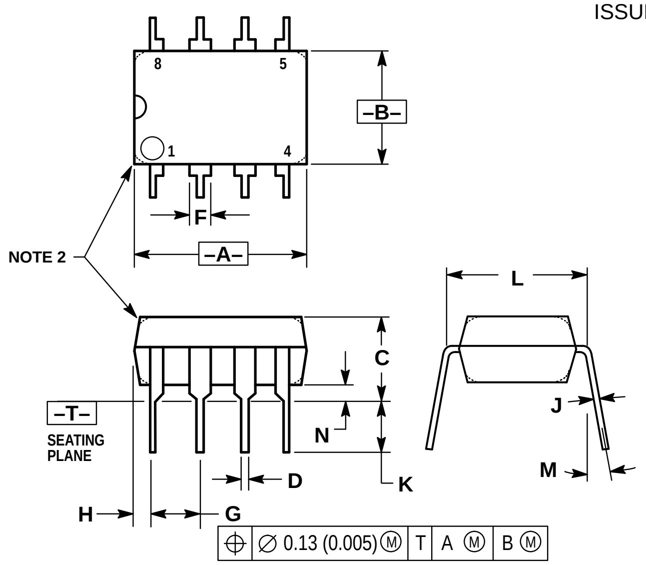
Figure 26. Split Supply Operation



NOTE: If V_{CC} and V_{EE} are not symmetrical about ground then FC1 must be connected through a capacitor to ground as shown on the front page.

OUTLINE DIMENSIONS

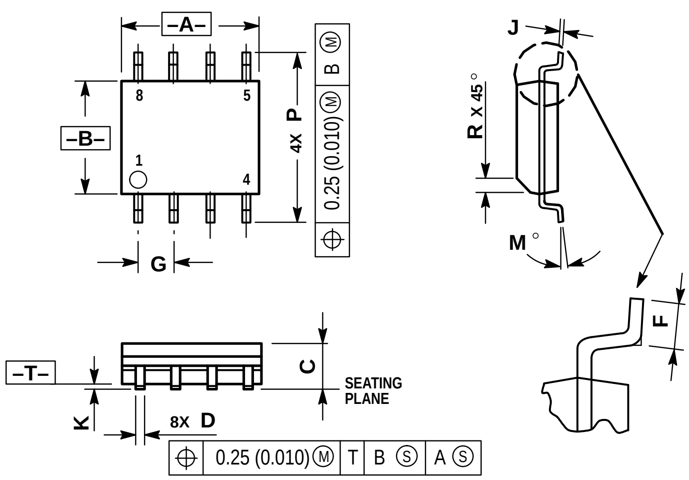
P SUFFIX
PLASTIC PACKAGE
CASE 626–05
ISSUE K



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

D SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SO–8)
ISSUE P

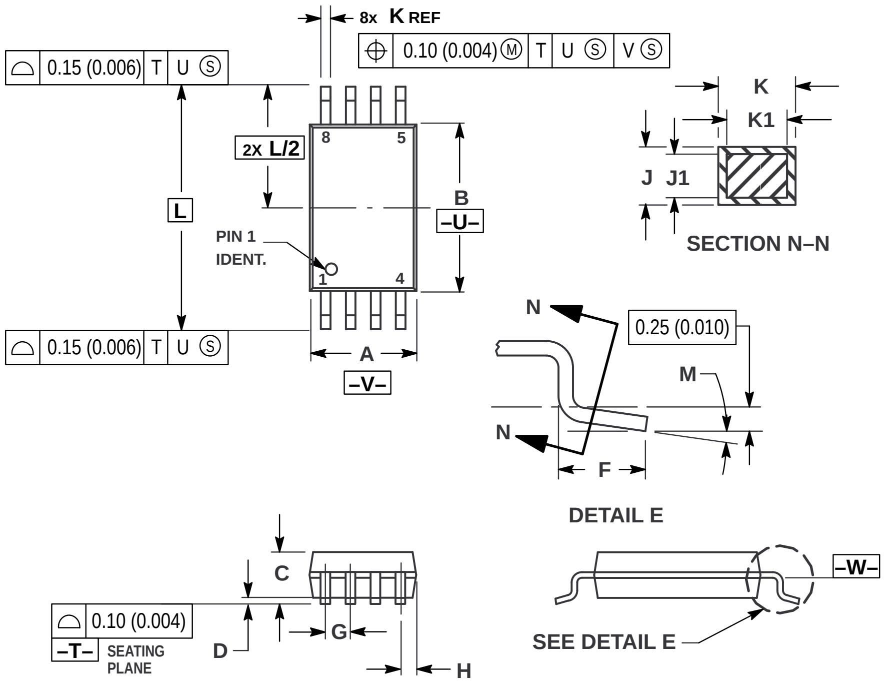


NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DIMENSIONS ARE IN MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
6. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.35	0.49
F	0.40	1.25
G	1.27 BSC	
J	0.18	0.25
K	0.10	0.25
M	0°	7°
P	5.80	6.20
R	0.25	0.50

OUTLINE DIMENSIONS

DTB SUFFIX
PLASTIC PACKAGE
CASE 948J–01
(TSSOP)
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

How to reach us:

USA / EUROPE / Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298